SERIES INTERCONNECTION OF SIX TRAPATT DEVICES ON A DIAMOND SUBSTRATE

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Abstract

The effects of package parasitics on series interconnections of TRAPATT diode chips on diamond substrates have been studied via time domain computer simulations and experiments at frequencies from 2 to 9 GHz. Guidelines for the selection of package parasitics have been identified, and multichip series configurations, employing six chips mounted thermally in parallel on diamond, have been successfully demonstrated at 7.5 GHz with 35.5 watts output power.

Introduction

Researchers have experimented with series connected TRAPATT diodes in the past and have succeeded in vertically stacking (thermally in series) such devices at frequencies from 1 to 9 GHz.[1,2,3,4] However, efforts to mount such devices thermally in parallel (side-by-side), as required for high power CW or long pulse applications, have not previously been successful above 5 GHz even though such configurations have been successfully demonstrated at 2 GHz.[3] Since vertical stacks of series connected diodes performed satisfactorily above 5 GHz while series diodes mounted side-by-side did not, it appears that the parasitic elements associated with he side-by-side mounting resulted in large reductions in combining efficiency.

This paper describes a new effort directed towards studying the device-circuit interaction via a computer simulation and application of the results of the study to solving the series TRAPATT diode problem above 5 GHz. Experiments and time domain computer simulations performed between 2 and 9 GHz have identified guidelines for the selection of diode package parasitics. Application of these guidelines to series connected diodes has resulted in combining efficiencies approaching 100% at frequencies up to 9 GHz. A multi-diode configuration with six chips mounted thermally in parallel and electrically in series on a diamond substrate yielded 35.5 watts at 7.5 GHz. Multi-chip diodes with two, three and four chips yielded 12, 14, and 21 watts respectively near 8.7 GHz.

Computer Simulation

The time domain computer simulation used to study the diode-circuit interaction was first used by John Carroll[5] and utilizes the simplified diode model shown in Figure 1. As suggested by Evans,[6] the diode is represented by a current pulse generator in parallel with the depletion layer capacitance of the diode. This model allows for concentration on the circuit and its interaction with the diode without becoming involved in the detailed device physics. The particle current generator h(t) is assumed to have a shape as shown in Figure 1. If the device is properly loaded for TRAPATT operation the voltage waveform v(t) will be similar to that shown. This classical TRAPATT voltage waveform consists of a large overvoltage having fast rise time to trigger the avalanche shock front, followed by a drop to zero and a recovery.

A typical circuit used in the time domain simulation is also shown in Figure 1. Representation of the diode particle current h(t) is normally accomplished graphically but can be performed analytically. The waveform is first broken into its harmonic components using the Fourier transform. The circuit impedance $Z(\omega)$ is then computed at the harmonic frequencies and used to calculate the voltage waveshape v(t) as shown. The calculated voltage waveforms are next analyzed with respect to rise time dv/dt of the triggering pulse, the peak voltage, and the time interval over which the voltage remains at a low value in order to determine compatibility with good TRAPATT voltage waveforms.

2 GHz Investigation

Initial experiments were conducted at 2 GHz using the diode mounting configuration shown in Figure 2 to study package parasitics. The configuration consisted of an alumina capacitor placed on a copper slug with a gold wire between the top of the capacitor and the top of the diode chip. A multi-slug coaxial test fixture with the center conductor contacting the capacitor was employed to evaluate the performance. Adjustments in the package capacitance were accomplished by changing capacitors, and the diode lead inductance was adjusted via the number and length of contact wires.

Variations in the lead inductance had relatively little effect on efficiency. On the other hand, experiments with the package capacitance revealed a drastic reduction of conversion efficiency for values greater than approximately 1 pf. Furthermore, it was determined that for the particular circuit and diode evaluated this maximum value of capacitance was related to the diode depletion layer capacitance such that C_p (max) $\simeq$ 2 $C_d(V_B)$ at 2 GHz. Computer simulations were performed at 2 GHz to verify these experimental observations. The model used is shown in Figure 1. Variations of the lead inductance, L, had little effect on the voltage waveforms as was observed experimentally, but the simulations with various capacitance values showed a strong dependence on capacitance and supported the experimental results. Above a maximum value of package capacitance the voltage waveforms lost their TRAPATT characteristics. This maximum value of capacitance agreed approximately with the experimental data.

Additional experiments were performed at 2 GHz using the series diode configuration of Figure 3. Previous experiments at the Naval Research Laboratory[3] had demonstrated that side-by-side series TRAPATT diodes combined efficiently at 2 GHz, but no data were available as to sensitivity to the package parasitics. The configuration of Figure 3 worked well at 2 GHz with no degradation in efficiency due to the series combination. In fact, the efficiency was higher in some cases than for a single diode, likely a result of the increased impedance level. The lead inductance between diodes was not critical, but a maximum value of package capacitance was found as before. With the series configuration the maximum package capacitance was related to the

series combination of the two diode depletion layer capacitances.

4 GHz Investigation

The frequency of the investigation was shifted upward in order to determine the frequency at which the combining efficiency of the series diodes began to deteriorate. Data indicated that a break frequency must exist since 2 GHz diodes readily combined while 8 GHz diodes had a combining efficiency of only about 50%. No degradation in efficiency was seen at 4 GHz with the series configuration.

6-9 GHz Investigation

Series experiments were next performed in the 6.0 to 7.5 GHz range where the combining efficiency was found to drop off rapidly above 7 GHz. Single diodes known to perform well over the 6 to 7.5 GHz range were connected in series in a manner similar to the configuration of Figure 3. For frequencies below 7 GHz the efficiency of the series pair was a high as that of the single diodes. However, attempts to tune the series diodes above 7 GHz resulted in efficiencies that were approximately one-half that of the single diodes.

Once again computer simulations were performed, this time at 6 GHz, to study the effect of package capacitance. These simulations again showed a maximum value of package capacitance which was related to the diode depletion layer capacitance. However, the maximum value was reduced for this higher frequency case such that $C_p(\max) \simeq 1.5\ C_d(V_B)$. This relationship was verified experimentally at 6 GHz with single diode chips in the manner described previously. Therefore, experiments were conducted to see if minimizing the package capacitance improved the series diode combining efficiency above 7 GHz. Little improvement was noted. However, in the process of these experiments at 7 GHz, it was observed that the location of the diode on the diamond metallization pad (as well as the point of contact of the grounding strap) had significant effect on performance. More detailed experiments indicated that the metallization pads on the .030 x .030 inch diamond surface were of sufficient size to behave as transmission lines at some high harmonic frequency. From Figure 3 it is evident, if one views the top surface of the diamond as a microstrip transmission line, that the "floating" diode has two parallel stubs extending from the lower diode terminal. Calculations indicated that these two open-circuited stubs, which were 0.015 inches long, should have impedances of 60-80 ohms, and that they were approximately one-eighth of a wavelength long at the 6th harmonic (42 GHz). This represents a reactance of approximately - j35 to ground between the two diodes. The harmonic shunt reactance could potentially be detrimental to the series connection and would tend to short the grounded diode. It should be stressed that these effects would be expected only at high harmonics since the metallization pads are much less than one-tenth of a wavelength long at the fundamental frequency and would certainly appear lumped for the first "few" harmonics.

Experiments were continued using small metallization pads which were merely large enough for mounting the diodes on the diamond. Also, the package capacitance was minimized with the use of a small quartz standoff for contacting. The efficiency of two series diodes mounted in this manner increased to approximately that of the single diode chip at frequencies up to 9 GHz and resulted in approximately 100% combining efficiency. Additional experiments verified that both minimum diamond metallization and minimum capacitance were necessary to achieve this 100% combining efficiency in the 7-9 GHz range. Omission of either of these conditions resulted in a combining efficiency of approximately 50%. The apparent significance of high harmonics ($\geq 5\ f_o$) on diode efficiency is certainly surprising and has been overlooked previously. Some sensitivity of diode performance to these harmonics was expected, but the 50% reduction in efficiency was not. To further verify the significance of this transmission line, an experiment was performed where the length of the metallization pad was varied from 30 mils to the size of the diode chip, carefully measuring efficiency at several lengths. These data showed that the maximum frequency of operation is inversely proportional to the pad length, with the best efficiency achieved at minimum length.

Multichip diodes with three, four and six series chips were fabricated to determine the limit to which chip level power combining could be extended at X-band. A micrograph of the six chip diode is shown in Figure 4. Contact to the diode was achieved with the copper post mounted in the center of the diamond. Performance of three multichip diodes is shown in Figure 5. The six chip device produced 35.5 watts output at 7.5 GHz. The individual chips were capable of 5-7 watts at this frequency. Other multichip configurations gave 12, 14 and 21 watts at 8.7 GHz with two, three, and four series chips respectively. These results indicate that little performance deterioration results from series connected diode chips at frequencies up to 9 GHz provided careful attention is given to the parasitics of the diode package.

Summary

The computer modelling and experiments have identified guidelines for the selection of TRAPATT diode package parasitics. Specifically, the shunt capacitance is particularily important and is limited by a maximum value which is related to the diode depletion layer capacitance, the frequency of operation and the specific circuit in which the diode is embedded.

The importance of high harmonic frequencies ($\geq 5\ f_o$) on conversion efficiency of X-band TRAPATT devices has been implied and necessitates special attention in the design of series connected multichip TRAPATT diodes. The feasibility of X-band chip level power combining with TRAPATT diodes has been demonstrated with the series connection of six diode chips which produced 35.5 watts output power.

Acknowledgements

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References

1. S. G. Liu and J. J. Risko, "Fabrication and Performance of Kilowatt L-Band Avalanche Diodes," RCA Rev., vol. 31, pp. 3-19, March 1970.

2. S. G. Lui, "2000 W-GHz Complementary TRAPATT Diodes," Presented at the Int. Solid State Circuits Conf., Feb. 15, 1973.

3. K. R. Gleason, C. T. Rucker, N. W. Cox, A. C. MacPherson, E. D. Cohen, "Experimental Study of Series Connected TRAPATT Diodes," IEEE Trans. on Microwave Theory and Techniques," vol. MTT-22, No. 8, pp. 804-806, August 1974.

4. "High Power I-Band TRAPATT Amplifier," Final Development Rept., NESC Contract No. N00039-72-C-0207, Project No. XF-52545011, 10 Sept. 1971 to 15 July 1973.

5. J. E. Carroll and R. H. Crede, "A Computer Simulation of TRAPATT Circuits," Int. J. Electronics, vol. 32, pp. 273-276, 1972.

6. W. H. Evans, "Circuits for High-Effiiency Avalanche Diode Oscillators," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-17, Dec. 1969, pp. 1060-1067.

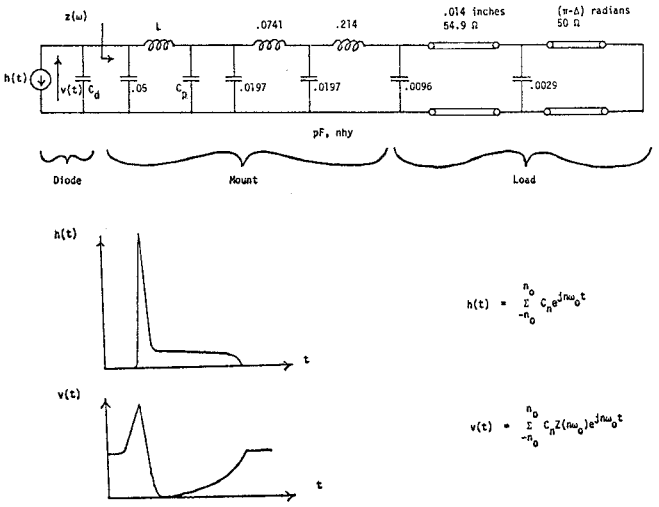

Figure 1. Diode and Circuit Model

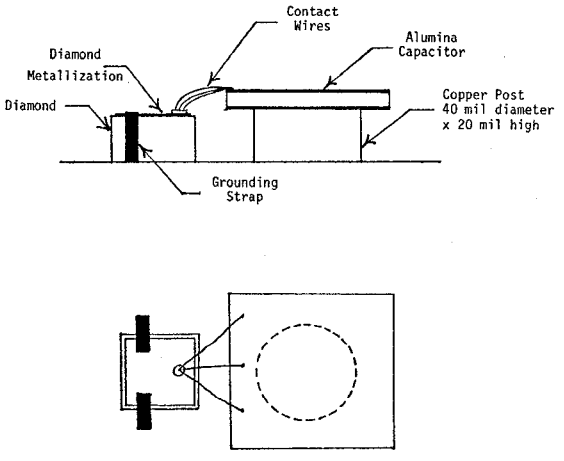

Figure 2. Diode Mounting Configuration

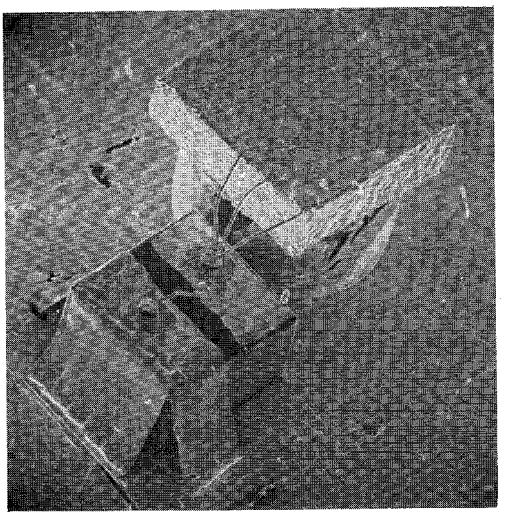

Figure 3. Two Series Chips on Diamond

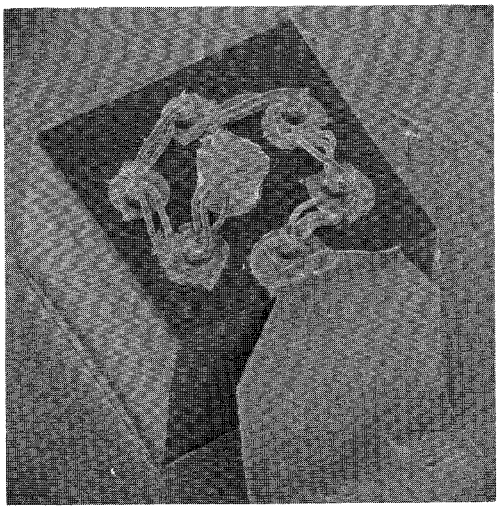

Figure 4. Six Series Chips on Diamond

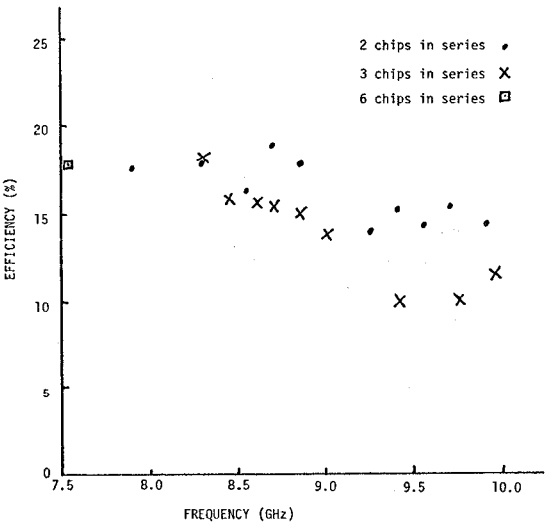

Figure 5. Multi-Chip Series Diode Performance